

Exciter ST5C

IEEE Std 421.5-2016 Exciter with static potential source

The diagram illustrates the control logic for the Exciter ST5C. It starts with a summing point (Σ) where V_{REF} is added and V_C is subtracted. This is followed by an HV gate and an LV gate, which take inputs from V_{SCLsum} , V_{UEL} , and V_{OEL} . The outputs of these gates are summed with V_S at another summing point. The resulting signal is then processed through two parallel paths, (a) and (b), each containing a transfer function block $\frac{1+sT_{C2}}{1+sT_{B2}}$ and $\frac{1+sT_{C1}}{1+sT_{B1}}$. The outputs of these paths are summed and then passed through a gain block K_R . The final output is E_{FD} , which is fed back through a gain block K_C and a transfer function $\frac{1}{1+sT_1}$ to the initial summing point. The diagram also shows various limits and feedback signals like V_{Rmin}/K_R , V_{Rmax}/K_R , and $V_T \cdot V_{Rmin}$.

States:

- 1 – E_{FD}
- 2 – Sensed V_T
- 3 – LL1
- 4 – LL2
- 5 – LLU1
- 6 – LLU2
- 7 – LLO1
- 8 – LLO2

alternate SCL input locations (V_{SCL})

- (1) summation point (voltage error)
- (2) take-over at voltage regulator input

alternate OEL input locations (V_{OEL})

- (1) summation point (voltage error)
- (2) take-over at voltage regulator input

alternate UEL input locations (V_{UEL})

- (1) summation point (voltage error)
- (2) take-over at voltage regulator input

footnotes:

- (a) Position B is selected when the UEL is active. Position A is used, otherwise.
- (b) Position B is selected when the OEL is active. Position A is used, otherwise.

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